DAVICOM Semiconductor, Inc.

DM8111XP

Low Power SoC With Integrated Image Recognition

DATA SHEET

Content

1   General Description

DM8111XP is a low power consumption SoC that built in black and white CMOS image sensor (CIS), simplified I/O interface and less external component count, made easily embedded and integrated various field applications. The recognition capability enables features such as: pedestrian detection, facial recognition, tracing, voice recognition for smart indoor/ outdoor applications.
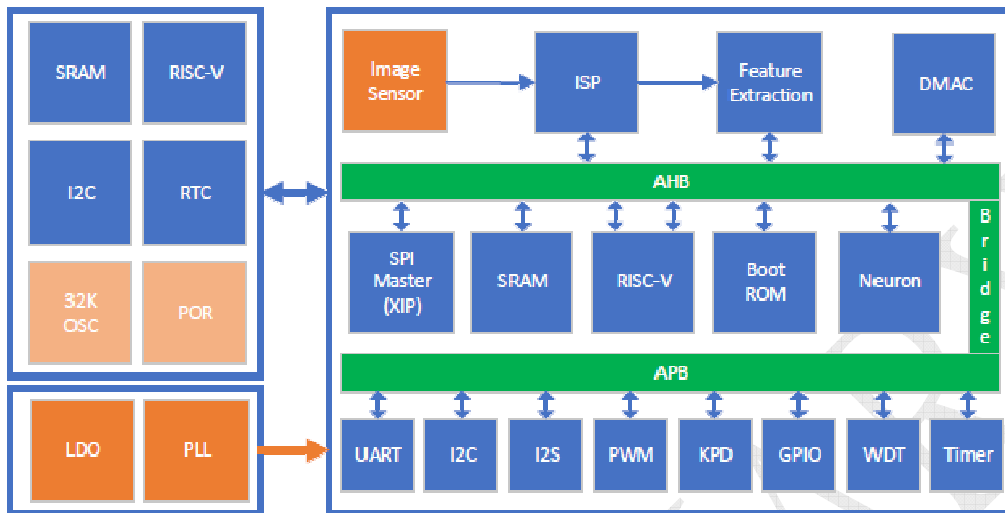
2   Features

- Integrated single chip SoC solution with CIS, image and voice recognition
- Built in B/W CIS (CMOS Image)
- Peripheral interface; SPI, UART, I2C, I2S, GPIO, Keypad
- Microphone and speaker interface for interactive control
- Adjustable 50/60 Hz flicker mitigation
- 288KB memory shared by all core
- Low power consumption
- Compact size at 6x4mm CSP package
- Operating temperature range 0℃~70℃
- 3.3V~4.2V regulator build-in

3   Application

- **Toy**
- **Facial Recognition**
- **Voice Recognition**
- **Machine Vision**
- **Tracking**
- **Smart Home (Lighting, Surveillance, Door Bell)**
- **Industry 4.0**
- **IP Cam**
- **Drone**
- **Robot**

4 Block Diagram

5 Specification

- **Sensor**
  - ➢ **Array Size: 320x320**
  - ➢ **Sensitivity: 3.0v/lux-sec**
  - ➢ **Pixel Size: 3µm x 3µm**
  - ➢ **Lens size: 1/13.3"**
- **Power Supply:**
  - ➢ **Battery: 3.0~4.8**
  - ➢ **I/O: 1.2V/3.3V**
- **Power Requirement:**
  - ➢ **Active: 120mA**
  - ➢ **Standby: 90µA**
- **Interfaces:**
  - ➢ **Standard: GPIO**
  - ➢ **Optional: I2C, SPI, Keypad, PWM**
- **Input Clocks:**
  - ➢ **24M Hz crystal**
  - ➢ **32.768 KHz crystal**
- **56-pin CSP package 6x4mm**

6 Pin Description

Pin No.	Pin Name	Type	Description
E2	RSTN	I	Reset input, active low, weak internal pull-up
B10	TM	I	Test mode control bit
F2	PORTB1	I/O	GPIO, Default: QSPI chip select, active low
E3	PORTB2	IO	GPIO, Default: QSPI clock input/output
F3	PORTB3	IO	GPIO, Default: QSPI serial input, bit0
E4	PORTB4	IO	GPIO, Default: QSPI serial input, bit1
F4	PORTB5	IO	GPIO, Default: QSPI serial input, bit2
E5	PORTB6	IO	GPIO, Default: QSPI serial input, bit3
E7	PORTB7	IO	GPIO, Default: SPI chip select, active low
F8	PORTA0	IO	GPIO, Default: SPI clock input/output
E8	PORTA1	IO	GPIO, Default: SPI serial input
F9	PORTA2	IO	GPIO, Default: SPI serial output
C1	PORTC0	IO	GPIO, Default: JTAG mode select
B1	PORTC1	IO	GPIO, Default: JTAG clock
D2	PORTC2	IO	GPIO, Default: JTAG data in
D3	PORTC3	IO	GPIO, Default: JTAG data out
E6	PORTC4	IO	GPIO, Default: First I2C clock input/output
F7	PORTC5	IO	GPIO, Default: First I2C serial data input/output
E9	PORTC6	IO	GPIO, Default: Strobe input
D9	PORTA3	IO	GPIO, Default: Second I2C clock input/output
D8	PORTA4	IO	GPIO, Default: Second I2C serial data input/output
C10	PORTA5	IO	GPIO, Default: UART interface input
C9	PORTA6	IO	GPIO, Default: UART interface output
C2	PORTA7	IO	GPIO, Default: JTAG Reset
A8	INTN	AI	Interrupt, active low
A2,C8	VBAT	P	Battery input
E1,F5,E10	VDDIO	P	1.2~3.3V I/O supply input
B8	VDDPK	AIO	Power keep LDO output
D1,F6,D10	VDD	P	1.2V digital core supply
B2	LX	AIO	Switch node for buck DCDC
C3	VFB	AI	Buck DCDC feedback, from VDD on PCB
B3	AVDDO	AO	CIS 2.8V analog LDO output

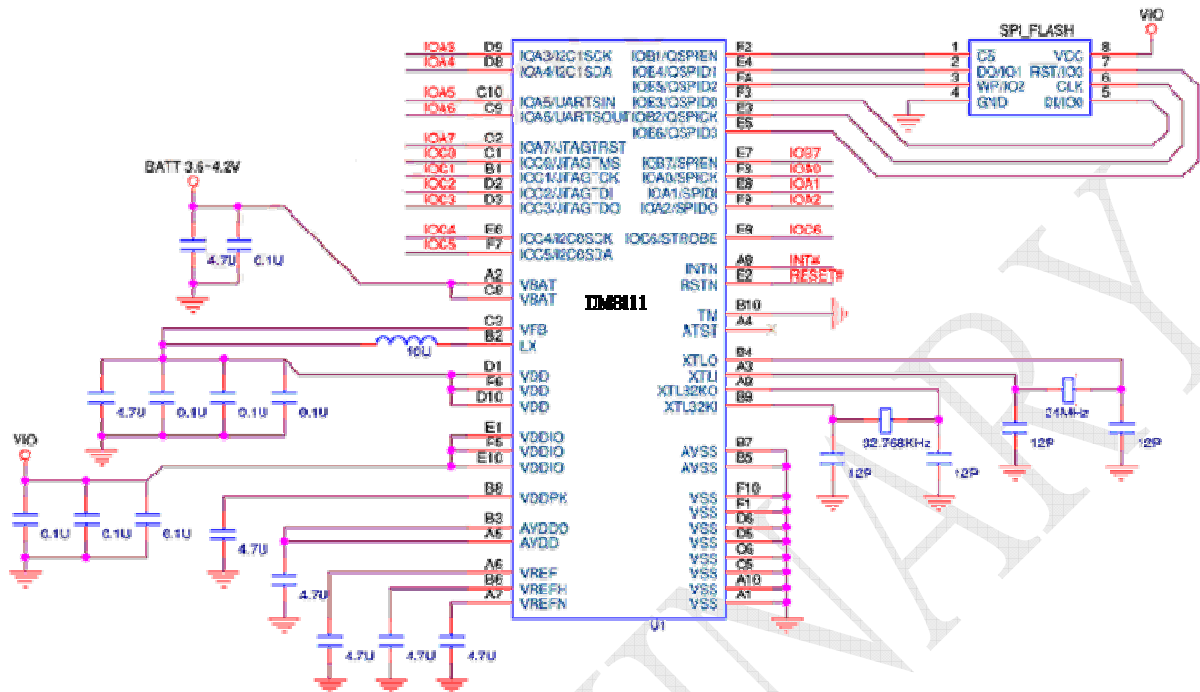| A5	AVDD	P	CIS 2.8V analog power input, connect to AVDDO on PCB
B5,B7	AVSS	G	CIS analog ground
B9	XTL32KI	AI	32kHz crystal input
A9	XTL32KO	AO	32kHz crystal output
A3	XTLI	AI	24MHz crystal input
B4	XTLO	AO	24MHz crystal output
A6	VREF	AIO	CIS reference voltage, connect a 1.0uF or larger capacitor to ground
B6	VREFH	AIO	CIS reference voltage, connect a 1.0uF or larger capacitor to ground
A7	VREFN	AIO	CIS reference voltage, connect a 1.0uF or larger capacitor to ground
A4	ATST	AO	Analog test pin
A1,A10,C5,C6, D5,D6,F1,F10	VSS	G	Digital ground

7   Absolute Maximum Ratings

Parameter	Rating
Battery (VBATT) voltage range	TBD
I/O (VIO) voltage range	TBD
Junction Operating Temperature	0℃ To 105℃
Ambient Operating Temperature	0℃ To 70℃
Storage Temperature	-50℃ To 150℃

8   Electrical Characteristics

Parameter	Comments	Min	Typ.	Max	Unit
VBATT	Battery supply input	3.3	3.6	4.2	V
VIO	I/O rail	1.2		3.3	V
VBATT supply current	Active @3.3V		110	130	mA
	Standby @3.3V		90		uA
VDD supply current	Active			200	mA
	Standby		TBD		mA
VIO supply current	Active		TBD		mA
	Standby		TBD		mA
V_{IH}	I/O pin input high level		TBD		V
V_{IL}	I/O pin input low level		TBD		V
V_{OH}	I/O pin output high level		TBD		V
V_{OL}	I/O pin output low level		TBD		V
R_{PU}	Reset pin internal pull-up resistance		TBD		Ω
I_{IL}	Input leakage current		TBD		µA
I_{OZ}	Tri-state output leakage current		TBD		µA
F_{SW}	Switching regulator frequency		1.5		MHz

9   Application Circuit

10 Application Information
10.1 Component Selection
10.1.1 Capacitor

Ideally each VBAT, VDD, and VIO input should have a dedicated 0.1uF decoupling capacitor. X5R dielectric should be chosen if stable performance over a wide temperature range is desired.

In addition, a 4.7uF+ decoupling capacitor is needed for the VBAT input and LX output after the inductor.

One 1.0uF+ decoupling capacitor is required for each VDDPK, AVDDO, AVDD, and VREF pins.

10.1.2 Inductor

DM8111XP uses a switching regulator to generate its own 1.2V internal core voltage. The switching inductor is external to the chip. Operating current is targeted at 200mA. For efficiency and noise performance, the inductor should satisfy the following requirements:

Parameter	Rating
Inductance	>4.7uH
Saturation current	>300mA
DC resistance	< 500mΩ

For example, Taiyo Yuden CBC2518T100 (10μH) and CBC2518T6R8 (6.8μH) satisfies these requirements in a small package. Choosing a smaller inductance value offers higher efficiency at the cost of higher ripple current.

If 1.2V core voltage is externally supplied, the inductor can be omitted. In this case, leave the LX and VFB pins floating. The external supply should budget up to 200mA for DM8111XP 1.2V core rail.

10.1.3 Crystal

Two crystals are required, one 32.768KHz and one 24.0MHz. (+/- 15 ppm)

10.1.4 Serial SPI Flash

The serial flash should support a minimum SPI clock speed of 10MHz. For faster boot time, dual- and quad-channel part should be selected. It should be large enough to contain the firmware and databases, but depends on the use case. Contact application team for guidance.
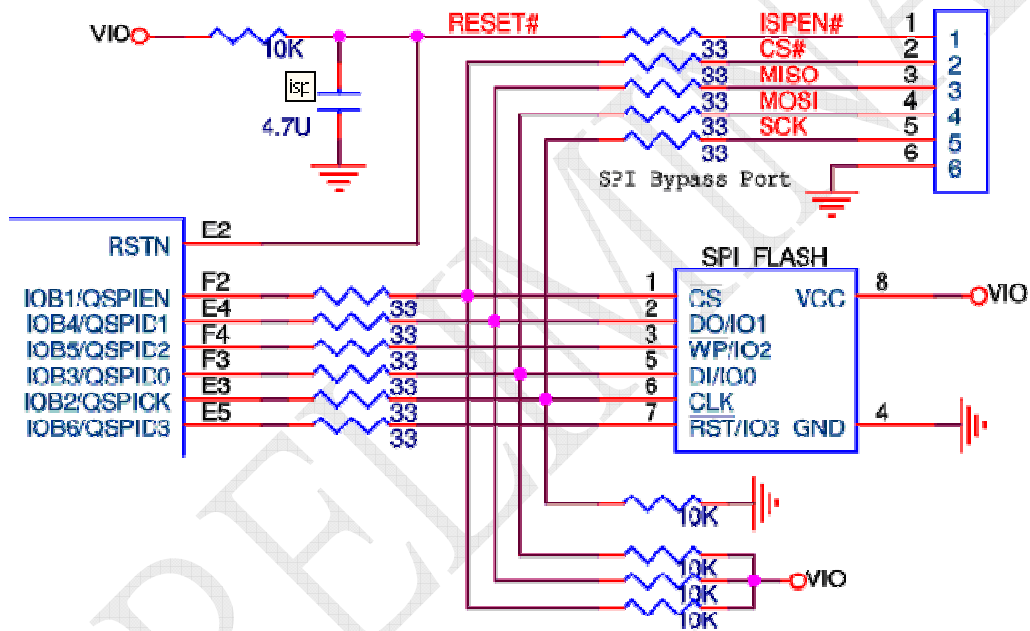
10.2 IN-SYSTEM-PROGRAMMING

Firmware and datasets are contained in the SPI serial flash. There are 2 ways to update the serial flash after module production.

10.2.1 Indirect

Indirect in-system-programming mode accesses the serial flash through I2C or SPI command interpreter on the DM8111XP. Tools are provided for this task.
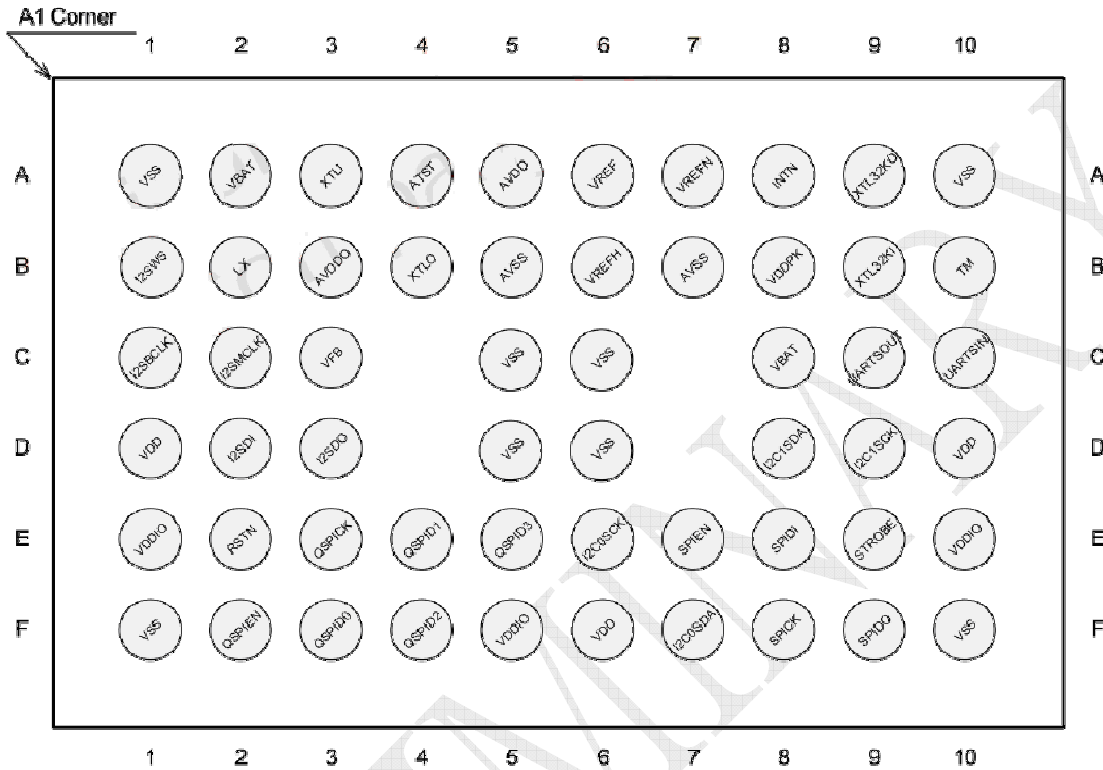
10.2.2 Direct

Direct in-system-programming is performed by placing the DM8111XP into reset mode which tri-states the SPI pins. This allows direct hardware access to the serial flash for much faster programming. Tools are provided for this task. Pull-up/down and series resistors are recommended if implementing direct ISP on-board.
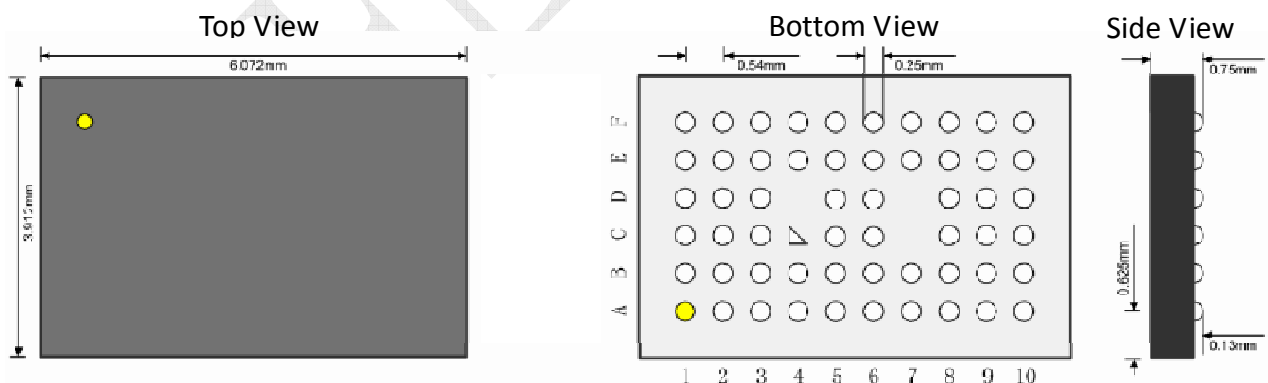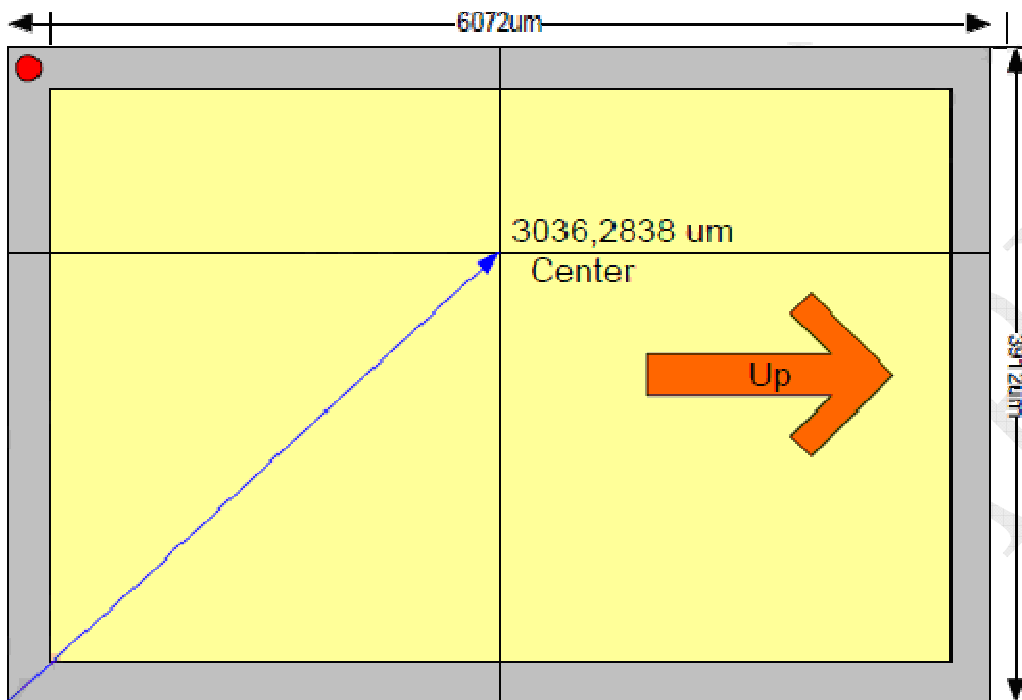
11 Package Information
11.1 BALL MAP

11.2 PACKAGE DIMENSIONS

Chip size: 6.072mm x 3.912mm
Pixel Array: 1.108mm x 1.024mm
Pixel center position: (3036um, 2838um), origin@left-bottom

11.3 PIXEL ARRAY CENTER

12 Ordering Information

Part Number	Pin Count	Package
DM8111XP	56	CSP package (6x4mm)

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DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.